CLAIMS

What is claimed is:

1) A method for reducing power in MRAM comprising:

(a) storing information in a RAM buffer;

(b) reading the information from the RAM buffer;

(c) writing the information to the MRAM;

(d) such that all storage cells connected to a selected wordline in the MRAM are written.

2) The method in Claim 1 wherein the RAM buffer is an SRAM buffer.

3) The method in Claim 1 wherein the RAM buffer is a DRAM buffer.

4) The method in Claim 1 wherein the RAM buffer is an array of flip-flops.

5) A method for reducing power in MRAM comprising:

(a) storing information from N write cycles in a RAM buffer;

(b) reading the information from the RAM buffer using fewer than N read cycles;

(c) writing the information to the MRAM using fewer than N write cycles;

(d) such that the number of power-up sequences required to write the information to the MRAM is reduced.

6) The method in Claim 5 wherein the RAM buffer is an SRAM buffer.

7) The method in Claim 5 wherein the RAM buffer is a DRAM buffer.

8) The method in Claim 5 wherein the RAM buffer is an array of flip-flops.

9) A method for reducing power in MRAM comprising:

(a) storing information from N write cycles in a RAM buffer;

(b) reading the information from the RAM buffer using one read cycle;

(c) writing the information to the MRAM using one write cycle;

(d) such that only one power-up sequence is used to write the information to the MRAM.

10) The method in Claim 9 wherein the RAM buffer is an SRAM buffer.

11) The method in Claim 9 wherein the RAM buffer is a DRAM buffer.

12) The method in Claim 9 wherein the RAM buffer is an array of flip-flops.

13) A system for reducing power in MRAM comprising:

(a) a RAM buffer;

(b) a MRAM;

(c) wherein the RAM buffer stores information;

(d) wherein the information stored in the RAM buffer is written to the MRAM such that all storage cells connected to a selected wordline in the MRAM are written.

14) The system in Claim 13 wherein the RAM buffer is an SRAM buffer.

15) The system in Claim 13 wherein the RAM buffer is a DRAM buffer.

16) The system in Claim 13 wherein the RAM buffer is an array of flip-flops.

17) A system for reducing power in MRAM comprising:

(a) a RAM buffer;

(b) a MRAM;

(c) wherein the RAM buffer stores information for N cycles;

(d) wherein the information stored in the RAM buffer is written to the MRAM in less than N cycles;

(e) wherein the number of power-up sequences required to write the information to the MRAM is reduced.

18) The system in Claim 17 wherein the RAM buffer is an SRAM buffer.

19) The system in Claim 17 wherein the RAM buffer is a DRAM buffer.

20) The system in Claim 17 wherein the RAM buffer is an array of flip-flops.

21) A system for reducing power in MRAM comprising:

(a) a RAM buffer;

(b) a MRAM;

(c) wherein the RAM buffer stores information for N cycles;

(d) wherein the information stored in the RAM buffer is written to the MRAM in one cycle;

(e) wherein only one power-up sequence is required to write the information to the MRAM.

22) The system in Claim 21 wherein the RAM buffer is an SRAM buffer.

23) The system in Claim 21 wherein the RAM buffer is a DRAM buffer.

24) The system in Claim 21 wherein the RAM buffer is an array of flip-flops.

25) A system for reducing power in MRAM comprising:

(a) a means for electronically reading and writing information;

(b) a MRAM;

(c) wherein the means for electronically reading and writing information stores information for N cycles;

(d) wherein the information stored in the means for electronically reading and writing information is written to the MRAM in less than N cycles;

(e) wherein the number of power-up sequences required to write the information to the MRAM is reduced.